Claims

[c1] 1.A circuit for identifying a defect location in a set of latches, said circuit comprising:

a first set of latches wired on a first wiring level;

a second set of latches wired on a second wiring level, each latch in the second set of latches being coupled with a corresponding latch in the first set of latches;

a controller that selectively parallel shifts the contents of the first set of latches into the second set of latches via a parallel shifting means;

a detector, coupled to an output of the second set of latches, that compares an output of the second set of latches with a predetermined bit sequence to identify a location of a defect in a defective set of latches, the defective set of latches being either the first or second set of latches, said detector further identifying whether a wiring of the defective set of latches is on the first wiring level or the second wiring level.

[c2] 2.The circuit of claim 1, wherein the defect location is a defect location, from a plurality of defect locations, that is closest to the output of the defective set of latches.

[c3] 3.The circuit of claim 1, wherein the defect location is a defect location, from a plurality of defect locations, that is farthest from the output of the defective set of latches.

[c4] 4.The circuit of claim 1, wherein the defective set of latches is laid out in a pre-determined matrix, such that identification of the defect location identifies a Cartesian coordinate of a physical location of the defect in a

circuit.

[c5] 5.The circuit of claim 1, further comprising means that, if the first and second sets of latches are both defective, parallel shift the contents between the first set of latches and a non-defective third set of latches wired on a third wiring level.

[c6] 6.The circuit of claim 1, wherein the defective set of latches contains a defect that prohibits a scan-in of data into all of the defective set of latches, wherein latches downstream of the defect contain data that do not correspond to the predetermined bit sequence.

[c7] 7.The circuit of claim 1, further comprising means for checking the parallel shifting means.

[c8] 8.A method for identifying a defect location in a set of latches, said method comprising:
scanning a first predetermined bit sequence into a defective first set of latches, the first set of latches being wired on a first wiring level;
parallel shifting the contents of the first set of latches into a second set of latches that is defect free, the second set of latches being wired on a second wiring level that is different from the first wiring level, wherein each latch in the second set of latches is coupled with a corresponding latch in the first set of latches;
scanning out the contents of the second set of latches; and
comparing the scanned out contents of the second set of latches with the predetermined bit sequence, whereby a bit sequence of the scan output identifies a location of a first upstream defect in the first set of latches

and a wiring level on which the first upstream defect occurs.

[c9] 9.The method of claim 8, further comprising:
scanning a second predetermined bit sequence into the second set of latches;
parallel shifting the contents of the second set of latches into the first set of latches;
scanning out the contents of the first set of latches; and
comparing the scan outputs of the first set of latches to identify a last downstream defect location in the first set of latches.

[c10] 10.The method of claim 8, wherein the predetermined bit sequence scanned into the first set of latches are all ones.

[c11] 11.The method of claim 8, wherein the predetermined bit sequence scanned into the first set of latches are all zeros.

[c12] 12.The method of claim 9, wherein the predetermined bit sequence scanned into the second set of latches are all ones.

[c13] 13.The method of claim 9, wherein the predetermined bit sequence scanned into the second set of latches are all zeros.

[c14] 14.The method of claim 8, wherein the location of the first upstream defect is determined by counting a number of scan shifts relative to the output of the second set of latches to determine the first upstream defect location in the first set of latches.

[c15] 15.The method of claim 9, wherein the location of the last downstream

defect is determined by counting a number of scan shifts relative to the output of the first set of latches to determine the last downstream defect location in the first set of latches.

[c16] 16.The method of claim 8, wherein the defective set of latches is laid out in a pre-determined matrix, such that identification of the defect location identifies a Cartesian coordinate of a physical location of the defect in a circuit.

[c17] 17.The method of claim 8, further comprising: testing a means for said parallel shifting for defects.

[c18] 18.A computer program product, residing on a computer usable medium, for identifying a defect location in a set of latches, said computer program product comprising:

program code for scanning a predetermined bit sequence into a first set of latches having a defect, said first set of latches being wired on a first wiring level;

program code for parallel shifting the contents of the first set of latches into a second set of latches that is defect free, said second set of latches being wired on a second wiring level, wherein each latch in the second set of latches is coupled with a corresponding latch in the first set of latches;

program code for scanning out the contents of the second set of latches; and

program code for comparing the scanned out contents of the second set of latches with the predetermined bit sequence, whereby a bit sequence

of the scan output identifies a first upstream defect location in the first set of latches.

[c19] 19.The computer program product of claim 18, further comprising:
program code for scanning a predetermined bit sequence into the second set of latches;
program code for parallel shifting the contents of the second set of latches into the first set of latches;
program code for scanning out the contents of the first set of latches; and
program code for comparing the scan outputs of the first set of latches to identify a last downstream defect location in the first set of latches.

[c20] 20.The computer program product of claim 18, wherein the predetermined bit sequence scanned into the first set of latches are all ones.

[c21] 21.The computer program product of claim 18, wherein the predetermined bit sequence scanned into the first set of latches are all zeros.

[c22] 22.The computer program product of claim 19, wherein the predetermined bit sequence scanned into the second set of latches are all ones.

[c23] 23.The computer program product of claim 19, wherein the predetermined bit sequence scanned into the second set of latches are all zeros.

[c24] 24.The computer program product of claim 18, wherein the location of

the first upstream defect is determined by counting a number of scan shifts relative to the output of the second set of latches to determine the first upstream defect location in the first set of latches.

[c25] 25.The computer program product of claim 19, wherein the location of the last downstream defect is determined by counting a number of scan shifts relative to the output of the first set of latches to determine the last downstream defect location in the first set of latches.

[c26] 26.The computer program product of claim 19, wherein the first and second sets of latches are on different wiring layers of a same integrated circuit.

[c27] 27.The computer program product of claim 26, further comprising program code for determining which layer of the different wiring layers is more defective that other wiring layers by counting the number of defective scan chains in each layer.

[c28] 28.The computer program product of claim 26, further comprising: program code for testing a means for said parallel shifting for defects.

[c29] 29.A method for identifying a defect location in a set of latches, said method comprising:
scanning a predetermined bit sequence into a first set of latches that is connection defect free, the first set of latches being wired on a first wiring level;
parallel shifting contents of the first set of latches into a second set of latches that has a defect, the second set of latches being wired on a

second wiring level, wherein each latch in the second set of latches is coupled with a corresponding latch in the first set of latches;

scanning out the contents of the second set of latches; and

comparing the scan output of the second set of latches with the predetermined bit sequence to identify a last downstream defect location in the second set of latches.